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Terms	Documents
(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	12

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Terms	Documents
(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	3

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Terms	Documents
(439/68 716/16 716/17 710/100 710/300 710/8 710/72 710/305 712/11 712/14 712/18 326/38 326/39 326/41).ccls.	9135

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<u>L3</u>	710/100,300,8,72,305;712/11,14,18;716/16,17;326/38,39,41;439/68.ccls.	9135	<u>L3</u>
	<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L2</u>	(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	3	<u>L2</u>
	<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L1</u>	(bus or sub-bus or subbus) same (DFP or FPGA or DPGA) same (programmable adj1 cell)	12	<u>L1</u>

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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

- ☐ 1. **Data-driven array processor for video signal processing**
Schmidt, U.; Caesar, K.; Himmel, T.;
Consumer Electronics, IEEE Transactions on
Volume 36, Issue 3, Aug 1990 Page(s):327 - 333
Digital Object Identifier 10.1109/30.103139
[AbstractPlus](#) | Full Text: [PDF](#)(616 KB) [IEEE JNL](#)
- ☐ 2. **Programmable logic machine (A programmable cell array)**
Skokan, Z.E.;
Solid-State Circuits, IEEE Journal of
Volume 18, Issue 5, Oct 1983 Page(s):572 - 578
[AbstractPlus](#) | Full Text: [PDF](#)(1176 KB) [IEEE JNL](#)
- ☐ 3. **Low power mixed signal microprocessor for programmable cell powered urinary incontinence stimulator**
Mouine, J.;
Electronics Letters
Volume 36, Issue 23, 9 Nov. 2000 Page(s):1913 - 1915
Digital Object Identifier 10.1049/el:20001346
[AbstractPlus](#) | Full Text: [PDF](#)(332 KB) [IEEE JNL](#)


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This paper appears in: **Solid-State Circuits, IEEE Journal of**
Publication Date: Oct 1983

Volume: 18, Issue: 5

On page(s): 572 - 578

ISSN: 0018-9200

Posted online: 2003-01-06 16:59:38.0

Abstract

The PLM is a single mask, programmable cell array with complete interconnect. It is 100% wireable and 100% testable with built-in LSSD. It achieves subnanosecond cell delay and 400-gate complexity with less than 1 W of power, and it is fabricated through a low-density process resulting in low cost and a four-day turnaround. This paper describes why the PLM was developed, its operational characteristics, and how it differs from conventional gate arrays.

Index Terms

Inspec

Controlled Indexing

Not Available

Non-controlled indexing

Bipolar integrated circuits Cellular arrays Integrated circuit technology Integrated logic circuits Large scale

Integration Bipolar integrated circuits Cellular arrays Integrated circuit technology Integrated logic circuits large

scale integration,

Author Keywords

Not Available

References

No references available on IEEE Xplore.

Citing Documents

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	U	I	Document ID	Issue Dat	Pages	Title	Current OR	Current XR
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6721830	20040413	31	I/O and memory bus system for DFPS and uni	710/100	710/305;
			B2					712/11;
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6513077	20030128	30	I/O and memory bus system for DFPS and uni	710/100	710/305;
			B2					712/11;
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6504398	20030107	28	Integrated circuit that includes a field-progra	326/41	326/39
			B1					
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6437441	20020820	56	Wiring structure of a semiconductor integrate	257/758	257/262;
			B1					257/365;
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6405299	20020611	51	Internal bus system for DFPS and units with two	712/11	712/10;
			B1					712/13;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6338106	20020108	30	I/O and memory bus system for DFPS and uni	710/100	712/11;
			B1					716/16
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6211697	20010403	28	Integrated circuit that includes a field-progra	326/41	326/39
			B1					
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6119181	20000912	23	I/O and memory bus system for DFPS and uni	710/100	710/110;
			A					712/11